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Invention: METHOD FOR FORMING A BIT LINE FOR A SEMICONDUCTOR DEVICE

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SPECIFICATION

METHOD FOR FORMING A BIT LINE FOR A SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for forming a bit line for a semiconductor device and, in particular, to an improved method for forming a bit line for a semiconductor device that also improves the contact process for the semiconductor device.

2. Description of the Background Art

If the minimum line width of a conventional DRAM cell is 'F', then the size of the unit cell will typically be approximately $10F^2$.

Recent work has led to suggestions for a method of reducing the cell size to $8F^2$. It appears that a cell size reduction from of $10F^2$ to a cell size of $8F^2$ may be achieved without fundamentally changing the conventional processes and concepts.

However, a new cell layout and process concept are required in order to reduce the cell size to $6F^2$. That is, using conventional methods, the cell size of $6F^2$ cannot be employed successfully for a highly integrated device.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method for forming a bit line for a semiconductor device that can be used to fabricate a highly integrated semiconductor device having a cell size of $6F^2$, by forming I-type active regions and a ladder-type bit line contacting the active regions in order to simplify subsequent contact processing.

In order to achieve the above-described object of the present invention, there is provided a method for forming a bit line for a semiconductor device, including the steps of: forming I-type active regions having a minimum line width on a semiconductor substrate, each active region being separated from adjacent active regions by the minimum line width distance; forming word lines having a minimum line width that are generally perpendicular to the I-type active regions, a pair of word lines crossing each I-type active region that leave three portions of the I-type active region exposed; forming a plug poly (polysilicon) on the active region between the word lines; forming an interlayer insulation film over the resultant structure; forming a bit line contact plug that overlaps the plug poly by a predetermined width; and forming a bit line having a minimum line width that overlaps the bit line contact plug by a predetermined width, the bit lines being oriented generally

perpendicular to the word lines and generally parallel to the I-type active regions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become better understood with reference to the accompanying drawings which are given only by way of illustration and thus are not limitative of the present invention, wherein:

Figures 1A to 1D are layout diagrams illustrating sequential steps of a method for forming a bit line of a semiconductor device in accordance with the present invention;

Figures 2A to 2F are cross-sectional diagrams illustrating sequential steps of the method for forming the bit line of the semiconductor device, taken along line I'-I" in Figure 1A; and

Figures 3A and 3B are cross-sectional diagrams illustrating sequential steps of the method for forming the bit line of the semiconductor device, taken along line II'-II" in Figure 1A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A method for forming a bit line of a semiconductor device in accordance with the present invention will now be described in detail with reference to the accompanying

drawings.

As illustrated in figure 1A, a device isolation film 300 for defining rows of active regions 200 is formed on a semiconductor substrate 100. Here, the active regions 200 have an I-type, or I-shaped, configuration having a minimum line width, and are separated in both the lateral and the longitudinal directions by the minimum line width. In addition, the rows of active regions 200 are aligned in the longitudinal direction with active regions in adjacent rows being offset by one third of the pitch in the longitudinal direction. Here, the pitch refers to the distance between one side of the active region and the corresponding side of a laterally adjacent active region.

Referring to Figure 1B, two word lines 400 are formed to cross the upper portions of each active region 200. Here, the word lines 400 are formed having the minimum line width and positioned to divide each active region into three portions. The word lines 400 have a stacked structure of a conductive layer 15 for the word line, a tungsten silicide layer 17 and a mask oxide film 19. Insulation film spacers 21 for the word line are formed at the sidewalls thereof.

Thereafter, a plug poly (not shown) designed to be positioned above and contact the active regions 200 is formed between the word lines 400.

An interlayer insulation film (not shown) is formed

over the resultant structure for planarization.

As shown in Figure 1C, a bit line contact plug 500 is then formed to overlap the plug poly above the active region 200 between the two word lines 400 by 30 to 70%.

As depicted in Figure 1D, a bit line 600 contacting the bit line contact plug 500 is then formed. Preferably, the bit line 600 is perpendicular to the word lines 400 and parallel to the rows of active regions 200. In addition, the bit line 600 overlaps the bit line contact plug 500 by 30 to 70%.

Figures 2A to 2E are cross-sectional diagrams illustrating sequential steps of the method for forming the bit line in a cell region, taken along line I'- I" in Figure 1A, and Figure 2F is a cross-sectional diagram illustrating the method for forming the bit line in a peripheral circuit region, taken along line I'- I" in Figure 1A.

As illustrated in Figure 2A, a device isolation film 13 for defining the active regions 200 is formed on the semiconductor substrate 100.

Referring to Figure 2B, a plug poly 23 is formed on the active regions 200 after forming word lines (not shown).

As shown in Figure 2C, an interlayer insulation film 25 is formed over the resultant structure.

As depicted in Figure 2D, a bit line contact hole exposing the plug poly 23 is formed, and a bit line contact

plug 27 is formed to fill up the bit line contact hole.

Here, the bit line contact plug 27 is overlapped with the plug poly 23 by 30 to 70%.

Referring to Figure 2E, a bit line 29 is formed to contact the bit line contact plug 27, and insulation film spacers 31 for the bit line are formed at the side walls of the bit line 29.

At this time, the bit line 29 is overlapped with the bit line contact plug 27 by 30 to 70%.

Figures 3A and 3B are cross-sectional diagrams illustrating sequential steps of the method for forming the bit line, taken along line II'-II" in Figure 1A. Here, the word lines 400 and the plug poly 23 are illustrated in more detail.

As illustrated in Figure 3A, the device isolation film 13 for defining the active regions 200 is formed on the semiconductor substrate 100.

The word lines are formed on the active regions 200 and the device isolation film 13.

Here, the word line 400 has a stacked structure of the conductive layer 15 for the word line, tungsten silicide layer 17 and mask oxide film 19. The insulation film spacers 21 for the word line are formed at the sidewalls thereof. The thickness of the mask oxide film 19 ranges from 3000 to 10000Å. A nitride film of similar thickness may be used

instead of the mask oxide film 19.

The plug poly 23 is formed on the active region 200 between the word lines 400.

As depicted in Figure 3B, the interlayer insulation film 25 is formed over the resultant structure. Here, a thickness of the interlayer insulation film 25 corresponds to 30 to 40% of the thickness of the mask oxide film 19.

Thereafter, the bit line contact hole exposing the plug poly 23 between the interlayer insulation films 25 is formed, and the bit line contact plug 27 is formed to fill up the bit line contact hole is formed.

As discussed earlier, in accordance with the present invention, the bit line is formed so that the bit line contact plug can be overlapped with the plug poly by a predetermined width, and thus a succeeding storage electrode contact process can be formed using a self aligned method.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiment is not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the metes and bounds of the claims, or equivalences of such

metes and bounds are therefore intended to be embraced by the appended claims.